

Application No.: 10/076003

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AMENDMENTS TO THE CLAIMS

The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1 – 19 (canceled)

20. (currently amended): An integrated circuit comprising:
a thin film transistor comprising
a deposition substrate;
a patterned first electrode layer formed adjacent the deposition substrate;
a second patterned electrode layer; and
a patterned polycrystalline organic semiconductor layer positioned between the patterned first electrode layer and the patterned second electrode layer,
wherein the patterned first electrode layer, the patterned organic semiconductor layer, and the second patterned electrode layer are each defined by a repositionable aperture mask, and
wherein one of the patterned first electrode layer and the patterned second electrode layer defines source and drain electrodes, and one of the patterned first electrode layer and the patterned second electrode layer defines a gate electrode.

21. (original): The integrated circuit of claim 20, wherein the patterned first electrode layer defines a gate electrode, and wherein the second patterned electrode layer defines source and drain electrodes.

22. (original): The integrated circuit of claim 20, wherein the patterned first electrode layer defines source and drain electrodes, and wherein the patterned second electrode layer defines a gate electrode.

23. (original): The integrated circuit of claim 21, wherein the source and drain electrodes are separated by a gap less than approximately 20 microns.

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24. (original): The integrated circuit of claim 23, wherein the gap is less than approximately 10 microns.

25. (canceled)

26. (currently amended): The integrated circuit of claim ~~25~~20, wherein the organic semiconductor is pentacene.

27. (canceled)

28. (currently amended): The integrated circuit of claim ~~27~~41, wherein the ~~complementary~~complimentary transistor circuit elements include a semiconductor layer comprising amorphous silicon.

29. (original): The integrated circuit of claim 20, wherein one or more of the layers include one or more interconnects.

30. (original): The integrated circuit of claim 20, further comprising one or more interconnect layers.

31. (original): The integrated circuit of claim 30, wherein the interconnect layers are defined by one or more repositionable aperture masks.

32. (original): The integrated circuit of claim 20, further comprising a patterned dielectric layer formed adjacent the organic semiconductor layer.

33. (original): The integrated circuit of claim 20, wherein the integrated circuit forms at least part of a circuit selected from the following group of circuits: an electronic display, a radio frequency identification (RFID) circuit, and an electronic memory.

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34 – 38 (canceled)

39. (previously presented): The integrated circuit of claim 20 wherein at least one of said first electrode layer, said patterned organic semiconductor layer or said second patterned electrode layer is vapor deposited.

40. (previously presented): The integrated circuit of claim 20 wherein each of said first electrode layer, said patterned organic semiconductor layer or said second patterned electrode layer are vapor deposited.

41. (new): An integrated circuit comprising:

(a) a thin film transistor comprising

a deposition substrate;

a patterned first electrode layer formed adjacent the deposition substrate;

a second patterned electrode layer; and

a patterned organic semiconductor layer positioned between the patterned first electrode layer and the patterned second electrode layer,

wherein the patterned first electrode layer, the patterned organic semiconductor layer, and the second patterned electrode layer are each defined by a repositionable aperture mask, and wherein one of the patterned first electrode layer and the patterned second electrode layer defines source and drain electrodes, and one of the patterned first electrode layer and the patterned second electrode layer defines a gate electrode, and

(b) one or more complimentary transistor circuit elements.